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**Code No: B7701/B6801**

**JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD**

**M. Tech I Semester Examinations, March/April 2011**

**VLSI TECHNOLOGY AND DESIGN**

**(EMBEDDED SYSTEMS AND VLSI DESIGN, VLSI & EMBEDDED SYSTEMS)**

**Time: 3hours** **Max. Marks: 60**

**Answer any five questions**

**All questions carry equal marks**

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1.a) Explain the fabrication steps for nMos Technology.
b) Explain the process of electron Beam Lithography. [6+6]

2.a) Discuss the significance of threshold voltage with input to fabrication parameters.
b) What is Latch up? How to prevent Latch up?
c) Draw the transfer characteristics of CMOS inverter and explain its operation. [12]

3.a) What is Buried contact? Compare it with Butting Contact.
b) Write design rules for wires.
c) How to scale the following parameters
i) Gate capacitance ii) Channel Resistance. [12]

4.a) What are the advantages of Domino logic? Draw the Domino OR gate and explains its operation with suitable waveforms.
b) Derive the equation for rise time of CMOS Inverter. [6+6]

5.a) What are the various simulation techniques for combinational networks? Explain them.
b) Draw the Wallace tree for four bit multiplier & explain its operation. [6+6]

6.a) Draw a circuit diagram for single transistor DRAM cell and explain. How it stock data?
b) How to optimize a power in sequential circuits? [6+6]

7.a) Write a short notes on off – chip connections.
b) Explain the principles of Architecture testing. [6+6]

8.a) Explain the different methods of scheduling.
b) Explain how a Hardware/Software co-design is used for chip designing. [6+6]

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